GigE Vision® IP core ALTERA

GigE Vision® compliant IP Core for Cyclone IV/V and Arria V devices

GigE Vision® is a standardized communication protocol for vision applications based on the well known Ethernet technology. It allows easy interfacing between GigE Vision® devices and PCs running TCP/IP protocol.

Sensor to Image offers a set of IP cores and a development framework to build FPGA-based products with Gigabit Ethernet interface.

In principle there are two possibilities to realize systems with Gigabit Ethernet interfaces:

– use processor with Gigabit Ethernet interface
– use hardware - based solution

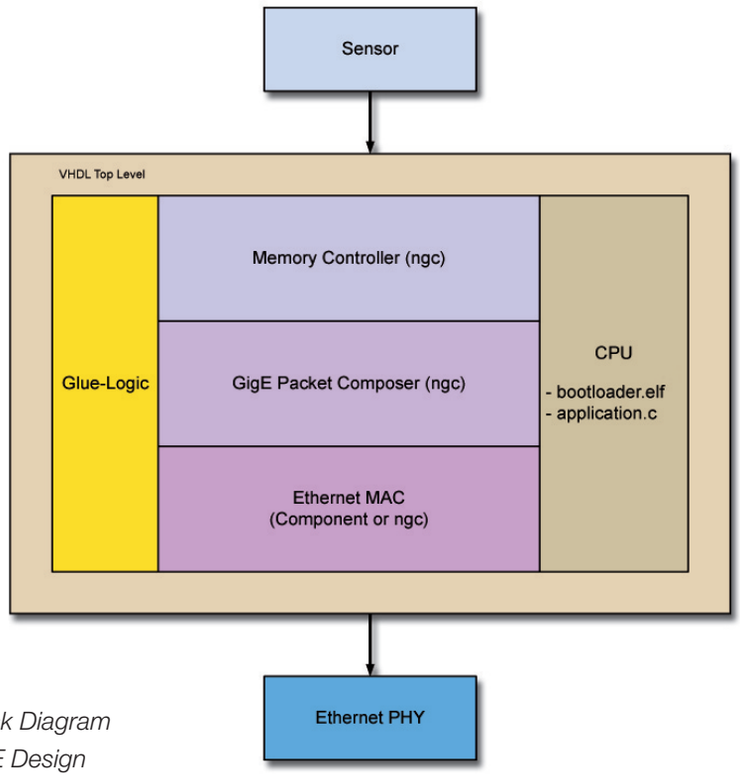
Sensor to Image developed a mixture of both concepts to combine advantages and avoid disadvantages of each approach.

This solution is made of a set of FPGA IP cores, which allows a maximum in performance at a small footprint and enough flexibility to realize custom solutions.

The following components are part of the design:

Top Level Design, which builds the interface between real hardware (e.g. sensor, external CPU, Ethernet Physical) and internal data processing. This module is delivered in source-code (VHDL), so it can be adapted and extended to custom hardware.

Memory Controller for different memory types, which allows frame buffering and image partitioning.



Block Diagram GigE Design

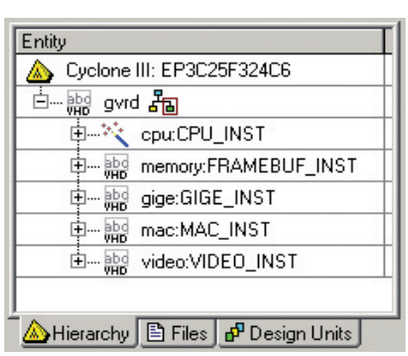
This is necessary to realize the packet resend function.

The **GigE Packet Composer** sends all data to the Ethernet MAC and realizes the high - speed “Streaming Channel” GVSP according to the GigE Vision® specification.

An **FPGA integrated CPU** (ARM or Nios® II processor) is for several non - time critical network and configuration tasks and it runs the “Control Channel” GVCP. Software is written in C and can be extended by the customer. Some software parts are delivered as compiled files only (e.g. bootloader, GigE-controller), other parts are in source code.

The delivered design framework comes with all necessary design files and cores, Quartus® project files and a Gigabit Ethernet camera and VGA-Out AddOn for the Altera® HSCMC - compliant FPGA boards, e.g. Cyclone® FPGA Starter. This system should be used as reference design and evaluation board.

As a development environment, Altera Quartus II software is used (not in scope of delivery).



Quartus® Project Tree

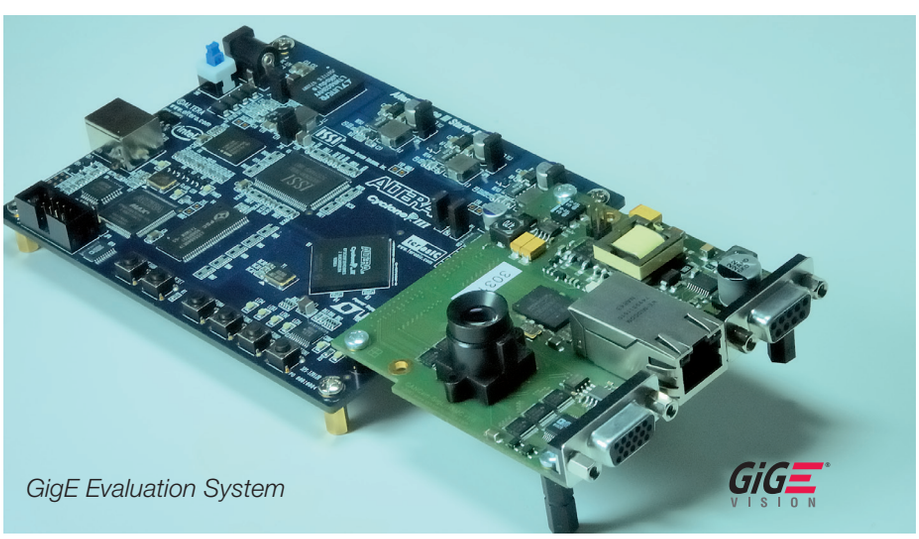
AVAILABLE MODULES

MODULE	COMMENT	CYCLONE® IV /V	ARRIA/STRATIX
Sync. bus as sensor interface	incl. 1 single tap sensor adaption incl. I²C/SPI core + C code	•	•
GigE Core	project licence for CPU interface, packet composer, MAC interface, packet resend including DDRx controller on AXI interface	•	•
Tri Mode MAC	Ethernet MAC core, only full-duplex supported	•	•
GigE Vision/GenICam software	SPHINX image viewer incl. filter driver, Transport Layer API, XML-File generation (separate product of Sensor to Image GmbH)	•	•
Full sources, design, ...	on request		

other FPGA vendors on request

RESOURCES

MODULE	CYCLONE® IV	STRATIX® IV	CYCLONE® V	ARRIA® V
GigE Packet Composer				
– Logig cells/ALMs	7074	3806	2734	2860
– Registers	4210	4558	4191	4321
– M9Ks	32	25	22	32
– DSPs	0	2	0	0
– PLLs	0	0	0	0
– Maximum clock frequency*	143 MHz	140 MHz	133 MHz	133 MHz
CPU system based on Nios II processor				
– Logic cells/ALMs	5214	2924	2901	3473
– Registers	3253	3473	3933	5021
– M9Ks	19	21	157	57
– DSPs	4	4	2	3
– PLLs	1	2	2	2
– Operating clock frequency	62.5 MHz	85 MHz	100 MHz	100 MHz
MAC				
– Logic cells/ALMs	1141	433	436	487
– Registers	698	526	681	760
– M9Ks	1	0	1	0
– DSPs	0	0	0	0
– PLLs	1	0	2	2
– Maximum clock frequency	125 MHz	125 MHz	125 MHz	125 MHz
* 80 MHz required to reach maximum bandwidth of Gigabit Ethernet				



GigE Evaluation System

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